Sub D1 C2

8. (Twice Amended) An apparatus for protecting a circuit from a transient event, comprising:

a signal transfer circuit arranged to receive a supply signal and output a first signal that powers the circuit during normal operation;

a charge storage circuit arranged to receive a bias signal and the first signal, the charge storage circuit providing a second signal that powers the circuit during the transient event; and

an inverting circuit arranged to receive the first signal, the second signal, and the bias signal, the inverting circuit coupled to a pin of the circuit, the inverting circuit arranged to hold the pin of the circuit high during a startup of the circuit, and low during the transient event and during normal operation.

Sub D1 C3

17. (Twice Amended) A method for rejecting a transient event from a circuit, comprising:

receiving a supply signal;

monitoring the supply signal for the transient event;

determining when the circuit is in normal operation, and when the transient event is occurring:

providing a first signal to power the circuit from a signal transfer circuit to a pin of the circuit when it is determined that the circuit is in normal operation, and

providing a second signal to power the circuit from a charge storage circuit that provides power to the pin of the circuit when it is determined that the transient event is occurring.

18. (Twice Amended) An apparatus for protecting a pin of a circuit during a transient event, comprising:

a means for receiving a supply signal;

a means for monitoring the supply signal to determine the transient event;

a means for determining when the circuit is in normal operation and when the transient event is occurring:

a means for providing a first signal to power the circuit from a signal transfer circuit to a pin of the circuit when it is determined that the circuit is in normal operation, and

a means for providing a second signal to power the circuit from a charge storage circuit that provides power to the pin of the circuit when it is determined that the transient event is occurring.

Please add new Claims 21-31 as follows:

21. (New) An apparatus for protecting a circuit from a transient event, comprising:

a signal transfer circuit arranged to receive a supply signal and output a first signal during normal operation to a pin of the circuit and to a charge storage circuit, wherein the signal transfer circuit comprises a transistor circuit having a body connection coupled to the pin of the circuit,; and

the charge storage circuit arranged to receive the first signal during normal operation and output a second signal to provide power during the transient event to the pin of the circuit, the charge storage circuit storing enough charge to provide the second signal during the transient event.

22. (New) The apparatus of Claim 21, wherein the charge storage circuit charges during normal operation, and discharges during the transient event.

23. (New) The apparatus of Claim 21, wherein the signal transfer circuit is further configured to prevent the stored charge of the charge storage circuit from falling below a level required to power the pin of the circuit.

24. (New) The apparatus of Claim 21, wherein the charge storage circuit comprises a capacitor circuit, the capacitor circuit storing enough charge to provide the second signal during the transient event.

25. (New) The apparatus of Claim 24, wherein the charge storage circuit is arranged to receive the first signal during normal operation and charge to the first signal during normal operation.

26. (New) The apparatus of Claim 21, wherein the transistor circuit, further comprises a first transistor and a second transistor arranged to prevent drain from the charge storage circuit.

27. (New) An apparatus for protecting a circuit from a transient event, comprising:

a signal transfer circuit arranged to receive a supply signal and output a first signal during normal operation;

a charge storage circuit arranged to receive a bias signal and the first signal, the charge storage circuit providing a second signal that provides power during the transient event; and

an inverting circuit arranged to receive the first signal, the second signal, and the bias signal, the inverting circuit coupled to a pin of the circuit, the inverting circuit arranged to hold the pin of the circuit high during a startup of the circuit, and low during the transient event and during normal operation, wherein the inverting circuit is a Schmidt trigger.

Cont C4

28. (New) The apparatus of Claim 27, wherein the charge storage circuit is a capacitor circuit.

29. (New) The apparatus of Claim 27, wherein the signal transfer circuit is a diode circuit.

30. (New) The apparatus of Claim 27, wherein the signal transfer circuit is a transistor circuit.

31. (New) The apparatus of Claim 30, wherein the transistor circuit, further comprises a first transistor and a second transistor arranged to prevent drain from the charge storage circuit.

REQUEST FOR RECONSIDERATION

Claims 1-20 are pending in the application. Claims 14-16 are allowed. Claims 1-6, 8, 10-12 and 17-19 are rejected. Claims 7, 9, 13 and 20 are objected to. Applicant respectfully requests reconsideration and allowance of all pending claims.

Claims 1, 8, 17, and 18 have been amended to further clarify the invention.

Claims 21-31 have been added to further define the invention. No new matter has been added and it is believed that no new search is required.

Objection of Drawings

The Office Action objected to some of the drawings because it is not believed that the transistors will turn off as described within the specification. It is maintained that the transistors will turn off as described within the specification. For further clarification please see discussion under the Objection to Specification section. Therefore, the FIGURES are correct as illustrated.

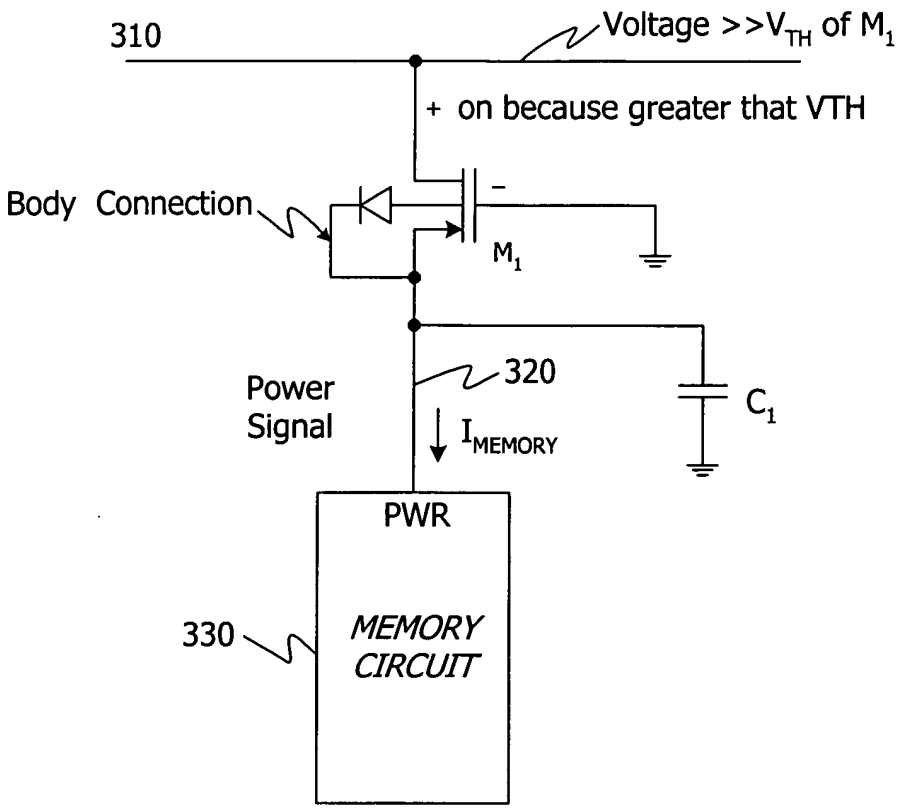
Objection to Specification

The Office Action requested clarification with respect to the operation of the circuit with respect to how transistor M1 of FIGURE 3 would turn off during a transient event.

Applicant has prepared examples to describe operation of an embodiment of the invention to aid the Examiner in understanding the operation of the circuit. Consider the schematic as illustrated in FIGURE 3.

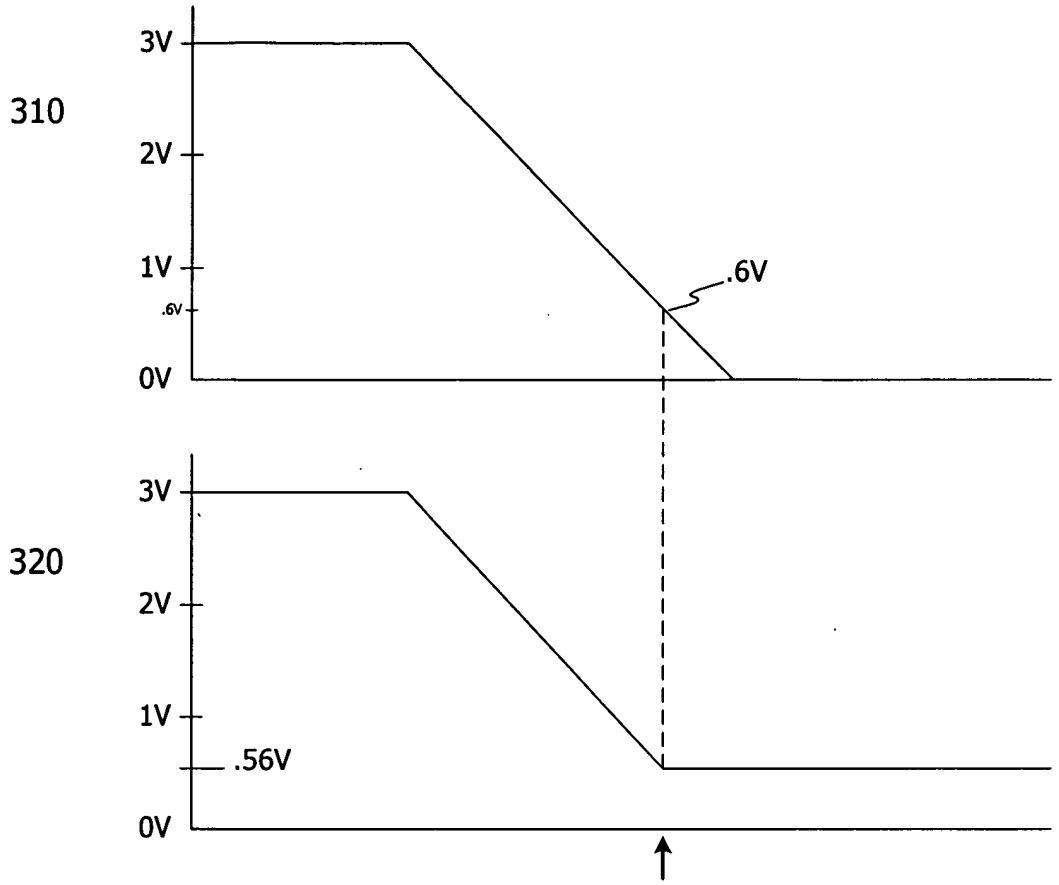
First, consider the situation when the supply signal is strong and well above the threshold voltage V_{TH} of the P-CHANNEL M_1.

Under these conditions:



Now, during this condition V_{DS} of the FET M_1 is close to zero because the current to the memory circuit is very low and the R_{ON} I_{MEMORY} product is near zero. M_1 is on hard. There is no current flow in the body diode.

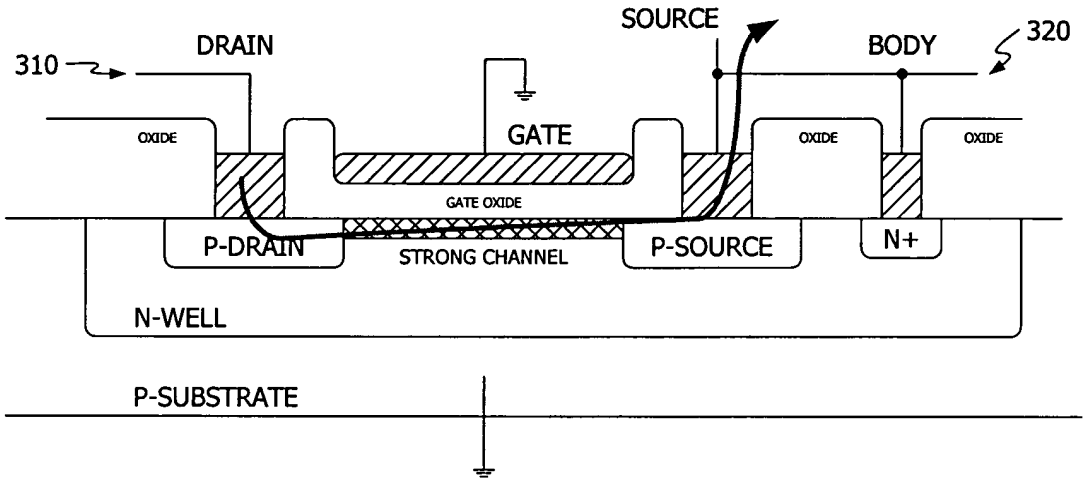
Now, consider the situation when the input voltage falls. The following are example waveforms:



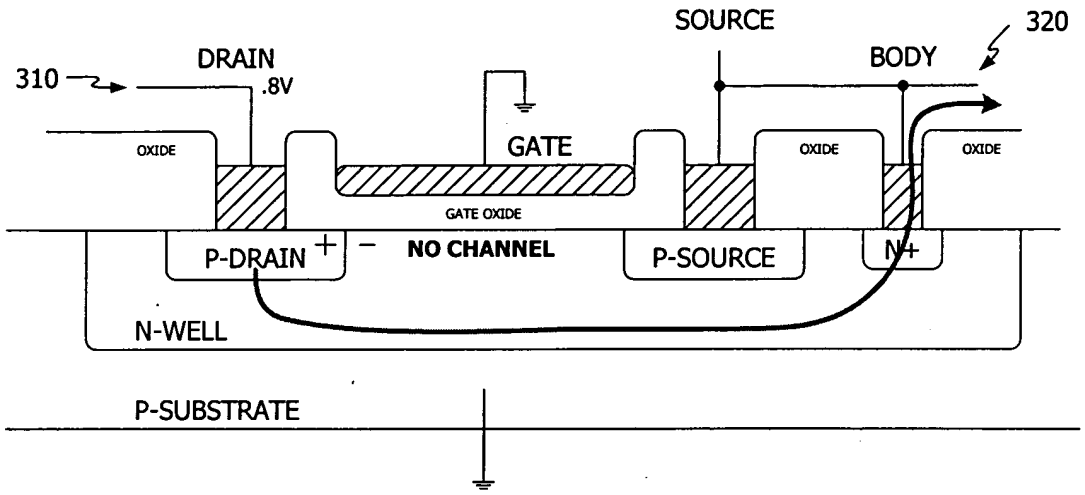
Node 320 is connected to the supply signal 310 for as long as the FET M1 is ON. Therefore, as the supply signal falls, Node 320 follows it down. Eventually, the voltage on 310 falls below the threshold voltage of the P-FET M_1 and the FET turns off. The P-N BODY diode may still be ON since the Vbe may be less than the threshold voltage and it will continue supplying current to Node 320 but at about 560mV at room temperature the diode stops supplying significant current to MEMORY CIRCUIT 330 because the BODY diode forward voltage is just too small. As Node 310 continues to fall, Node 320 is held up by capacitor C1. According to one embodiment, at these voltages, the current demand from the MEMORY CIRCUIT is almost nil and the voltage on 320 stays at about .5V, enough to hold the latch on.

Capacitor C1 is slowly discharging from the leakage of the MEMORY CIRCUIT and the reverse-biased BODY diode. The memory is held on and the information in the memory is preserved for a limited amount of time depending on the size of the capacitor and the leakage current.

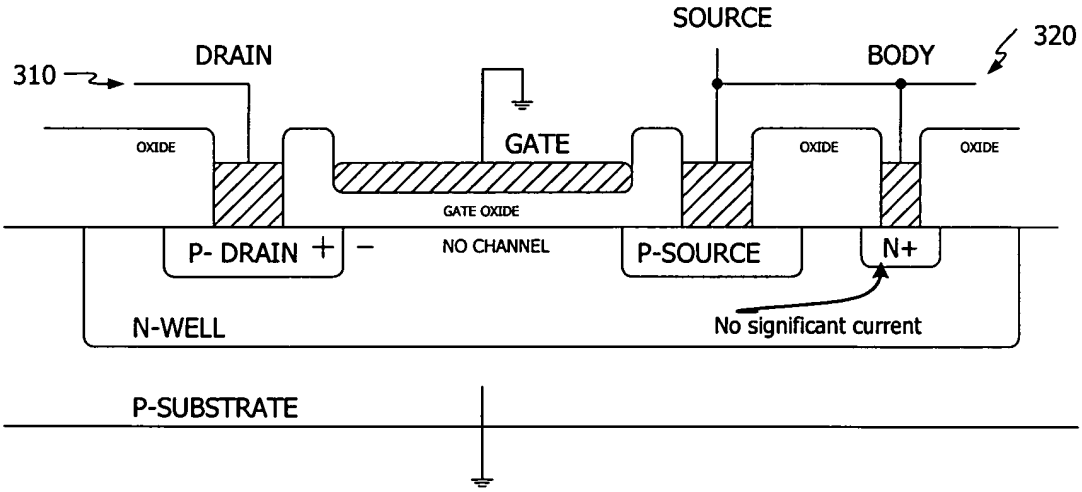
It may also be instructive to look at a cross section of a FET during four voltages cases. The cross section illustrated is of a typical PMOS device constructed in a N-well on a P-substrate.



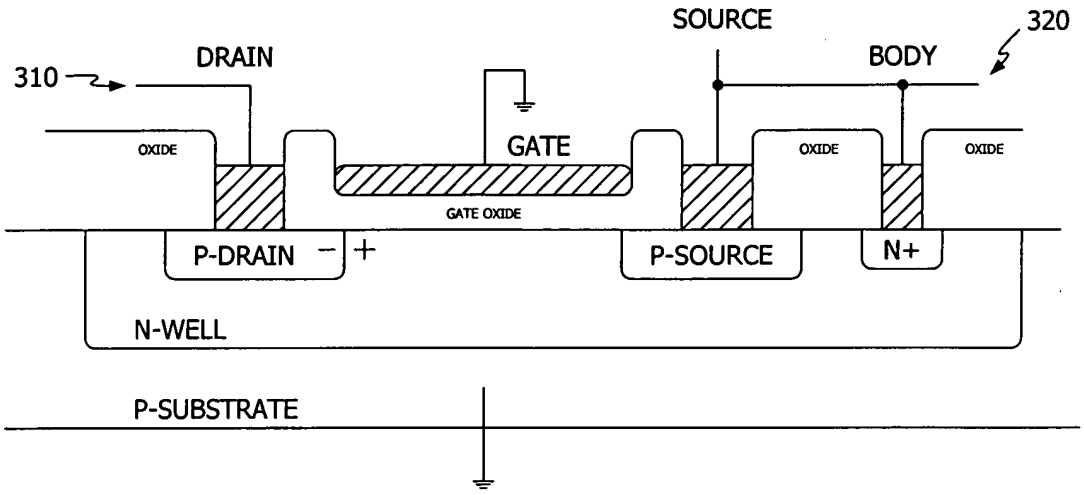
CASE 1: The voltage between 310 and the GATE (GND) is greater than the threshold voltage V_{TH} and the FET is ON. V_{DS} is $\approx$ 0V so, $V_D \approx V_S$ = N-WELL (BODY).



CASE 2: No CHANNEL, $V_{GD} < V_T$ but BODY diode is ON and supplying current to Node 320.



CASE 3: Node 310 is above ground but no current flows between 310 and 320 because forward voltage of DRAIN to BODY is not sufficient to allow much current flow.



CASE 4: Node 310 is at or just below ground. The P-DRAIN to N-WELL diode is reverse-biased; the N-WELL is at the potential of the CAP C_1. The P-SUBSTRATE is at ground so no current flow into N-WELL since the junction is still reverse-biased.

The Office Action also requested clarification with regard to transistors M1 and M2 function and how the may be replaced by a single diode (See Specification, Page 7, Lines 10-11). As illustrated in the figures, transistors M1 and M2 are P-channel FETs. According to one embodiment, transistors M1 and M2 are "used to help ensure that the channel-body diode does not drain current from capacitor C1. Using back-to-back transistors with the body connection connected to the source helps to ensure that any charging or discharging of capacitor C1 through the body path of the transistors is prevented." (Specification, Page 7, lines 5-9). Additionally, "[d]uring normal operation, transistors M1 and M2 are on (conducting) and are arranged to provide a power signal at node 320 received by capacitor C1 and the PWR pin of memory circuit 330." (Specification, Page 6, lines 27-29). Therefore, it is clear that a single diode may be used to replace transistors M1 and M2.

The Office Action has also requested clarification with regard to the circuits shown in FIGURES 5-7 and 10. It is believed that the above discussion has clarified the operation of the circuit and no further discussion is needed.

Newly added Claims

Claims 21-31 have been added to further define the invention. Claim 20 has been rewritten in independent form as Claim 21 to include the limitation of base Claim 1. Claim 9 has been rewritten in independent form as Claim 27 to include the limitation of base Claim 8. Therefore, it is believed that Claims 21and 27 are allowable as written. Thus, newly added Claims 22-26 and 28-31 should also be allowable since they depend on valid base claims.

Objection of Claims

The Office Action objected to Claims 8-13 because of an informality. Specifically, "the" was missing before the second reference to "second signal" on line 7 of Claim 8 (Office Action, Page 5, last paragraph).

In response, Claim 8 has been amended to overcome the objection.

Rejection of Claims under 35 U.S.C. §103(a)

The Office Action states that "charge storage circuit C2 will provide its stored charge (e.g. equivalent to the fully charged, stable level of Vdd) as the second signal to provide power (e.g. voltage) to pin A of circuit 3 during the transient event. Therefore, it would be obvious to one of ordinary skill in the art that circuit 3 would be considered protected from a sudden, short transient event, thus rendering claims 1 and 2 obvious." (Office Action, Page 7, first paragraph)

Applicant respectfully disagrees. Circuit 3 illustrated in Tailliet is not protected from a transient event. Circuits 4, 5, and 6 in Tailliet receive their power from Vdd, not from pin A. Therefore, during a transient, the drop in Vdd may cause circuits 4, 5, and 6 to operate incorrectly, thus changing the value of the POR signal. Even though there may be a signal at pin A, it is clear that this signal is not being used to power circuit 3 (or circuits 4, 5, or 6), and therefore circuit 3 is not protected from a transient event.

The Office Action also states that "one of ordinary skill in the art would know that capacitor circuit C2 would be sufficient in size to hold enough charge during a transient event...otherwise circuit 3 could inadvertently switch its logic state during the transient event." (Office Action, Page 7, last paragraph). Applicant respectfully disagrees. It is clear that capacitor circuit C2 illustrated in Tailliet is not sized to store enough charge during a transient event to provide power to circuit 3. Tailliet shows a POR circuit, where capacitor C2 is sized such that the circuit will operate properly upon a POR. This is not sized for supplying power to circuit 3 during a transient event. As discussed above, circuit 3 comprising circuits 4, 5, and 6 is NOT powered by the signal supplied at pin A. Additionally, the circuit illustrated in Tailliet is not protected from a transient, and circuit 3 can "inadvertently switch its logic state during the transient event" thereby changing "the level of the POR output signal when it isn't necessary." (Office Action, Page 7, bottom of page)

Applicant has amended Claim 1 to further clarify the invention. As amended, Claim 1, recites, in part "wherein the circuit is powered by the first signal during normal operation" and "wherein the circuit is powered by the second signal during the transient event."

Tailliet, on the other hand, does not power circuit 3 through a signal transfer circuit and charge storage circuit. As discussed above, and can be seen by referring to FIGURE 2 in

Tailliet, circuit 3 is powered from Vdd. Circuit 3 in Tailliet is used for tracking a signal and is protected from a transient.

Claim 8 has been amended to clarify the invention. As amended, Claim 8, recites in part, "a first signal that powers the circuit during normal operation;" and "providing a second signal that powers the circuit during the transient event."

Claims 17 and 18 have been similarly amended.

The Office Action states that Tailliet's power signal "can be considered a power supplied to Tailliet's overall circuit." Applicant respectfully disagrees. As amended, the claims clearly show that the signals provided to the circuit are used to power the circuit. As discussed above it is clear that the signal at pin A of circuit 3 is not used to power circuit 3.

For at least the reasons discussed above, applicant respectfully submits that independent Claims 1, 8, 17, and 18, as amended, are not obvious in view of the references cited in the Office Action and are, therefore, allowable. Claims 2-7, 9-13, and 19 and 20 are dependent from valid base claims, and therefore include the limitations of the base claims. Therefore, Claims 2-7, 9-13, and 19 and 20 are allowable for at least the same reasons.

Additionally, it is believed that newly added Claims 21-31 are allowable as they include the limitations of allowable base claims as indicated within the Office Action.

Conclusion

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application,

the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Attached to this response are pages entitled "MARKED VERSION SHOWING CHANGES" that illustrate the changes made to the paragraphs and claims amended above.

Respectfully Submitted,

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